Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1 and 49-53, 55-60, and 65-70 are pending in the application, with 1, 49, and 65 being the independent claims. Claims 2-48, 54, and 61-64 have been canceled without prejudice to or disclaimer of the subject matter therein. New claims 65-70 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Double Patenting Rejection

On page 2, paragraph 1 of the Office Action, the examiner indicated that it was unclear whether a new terminal disclaimer had been filed in the present application or a copy from a parent application. The Examiner further indicated that if a copy from a parent application had been filed in the present application, a new terminal disclaimer may be required. Attached hereto is a duplicate copy of the disclaimer filed in the present application. The terminal disclaimer filed was a new terminal disclaimer and not a copy from a parent application. Accordingly, reconsideration and withdrawal of all obviousness-type double patenting rejections are respectfully requested.

Rejections under 35 U.S.C. § 101

Beginning on Page 2, paragraph 2 of the Office Action, the Examiner rejected claims 1, 49, and 52 under 35 U.S.C. § 101 for allegedly being directed to non-statutory subject matter. Applicants respectfully disagree that the claims are directed to non-statutory subject matter. However, in order to expedite prosecution and allowance of the present application, Applicants has amended all of the pending claims to convert them from method claims to structure claims directed to a microprocessor. For example, claim 1 as amended now recites:

> 1. A microprocessor having a plurality of registers, comprising:
> a first processing unit that
> in response to a first load instruction loads a first plurality of data bytes into a first register,
> in response to a second load instruction loads a second plurality of data bytes into a second register, and
> in response to an alignment instruction determines a starting data byte in the first register, wherein the starting data byte specifies a first data byte of an aligned vector, extracts the aligned vector from the first register and the second register beginning from a first bit in the starting byte of the first register continuing through bits in the second register, and replicates the aligned vector into a third register such that the third register contains a plurality of data elements aligned for single instruction multiple data (SIMD) processing; and
> a SIMD processing unit coupled to the first processing unit that operates on the aligned vector.

Support for the claim amendments is found throughout the entire written specification and drawings of the present application, as well as in the original claims. See, for example, FIGS. 3-6 of the present application and the written description thereof, the description of the alignment instruction that begins on page 14 of the present

application, and the description of the shuffle instruction that begins on page 17 of the present application.

The claims as amended are directed to statutory subject matter (i.e., a microprocessor). Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Rejections under 35 U.S.C. § 103

Beginning on page 3, paragraph 4 of the Office Action, the Examiner maintained and incorporated by reference the obviousness rejection set forth in the Office Action dated August 8, 2005. This rejection was based on U.S. Patent No. 5,887,183 to Agarwal et al. ("Agarwal") in view of U.S. Patent No. 5,922,066 to Cho et al. ("Cho"). Applicants respectfully traverse this rejection.

As noted above, Applicants maintain that the previously presented claims were directed to statutory subject matter and are patentable over the art of record. However, in order to expedite prosecution and allowance of the present application, Applicants have amended all of the pending claims. The amendments are being made to change the statutory class of the claimed invention from method to apparatus without intending to narrow the scope of the claims.

As amended, independent claim 1 recites a microprocessor having "a plurality of registers" and "a first processing unit" that "in response to an alignment instruction determines a starting data byte in the first register, wherein the starting data byte specifies a first data byte of an aligned vector, extracts the aligned vector from the first register and the second register beginning from a first bit in the starting byte of the first

register continuing through bits in the second register, and replicates the aligned vector into a third register such that the third register contains a plurality of data elements aligned for single instruction multiple data (SIMD) processing." Independent claim 49, as amended, recites a microprocessor having "a plurality of registers" and "a first processing unit" that "in response to a shuffle instruction reads a first plurality of data elements from the first register and a second plurality of data elements from the second register, and writes the first plurality of data elements and the second plurality of data elements into a third register in a particular order specified by the shuffle instruction to produce a vector having a plurality of data elements aligned for single instruction multiple data (SIMD) processing." These recited features of independent claims 1 and 49 are neither taught nor suggested by Agarwal. Cho does not overcome the deficiencies of Agarwal. Thus, independent claims 1 and 49 are patentable over Agarwal and Cho, alone and/or in combination.

Dependent claims 50-53, and 55-60 depend from one of independent claims 1 and 49, and are patentable over Agarwal and Cho, alone and/or in combination, for at least the same reasons provided herein with respect to independent claim 1 and/or independent claim 49, and further for the specific features they recite.

Reconsideration and withdrawal of this rejection are respectfully requested.

New Claims 65-70

Applicants have added new claims 65-70. Claim 65 is an independent claim that recites features similar to independent claims 1 and 49. Accordingly, new independent claim 65 is patentable over Agarwal and Cho, alone and/or in combination, for reasons

similar to those provided herein with respect to independent claim 1 and independent claim 49. New claims 66-70 depend from independent claim 65 and are patentable over Agarwal and Cho, alone and/or in combination, for reasons similar to those provided herein.

Favorable consideration and allowance of new claims 65-70 are respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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